UNIT IV

FET Biasing

INTRODUCTION

The biasing levels for a silicon transistor configuration can be obtained using the characteristic equations $V_{BE} = 0.7$ V, $I_C = \beta I_B$, and $I_C \cong I_E$. The linkage between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, while nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have a graphical orientation rather than direct mathematical techniques.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A} \tag{1}$$

and

$$I_D = I_S \tag{2}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2 \tag{3}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \tag{4}$$

It is particularly important to realize that all of the equations above are for the *device only!* They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

1. FIXED-BIAS CONFIGURATION

e simplest of biasing arrangements for the *n*-channel JFET appears in Fig. .1. Referred to as the fixed-bias configuration, it is one of the few FET configurations thatcan be solved just as directly using either a mathematical or graphical approach. Bothmethods are included in this section to demonstrate the difference between the twophilosophies and also to establish the fact that the same solution can be obtained us-ing either method.

The configuration of Fig. 6.1 includes the ac levels $\ddot{O}_i$ and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 9). For the dc analysis,

$$I_G \cong 0 \text{ A}$$

and

$$V_{R_G} = I_G R_G = (0 \text{ A})R_G = 0 \text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 2 specifically redrawn for the dc analysis.

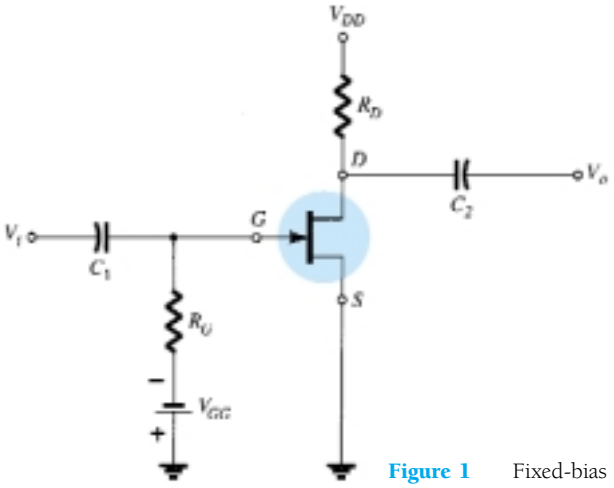


Figure 1 Fixed-bias configuration.

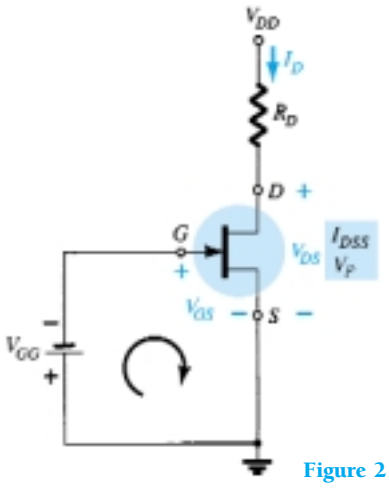


Figure 2 Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the de- fined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly op- posite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction ofthe indicated loop of Fig. .2 will result in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \tag{5}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in notation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation: the

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 6.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

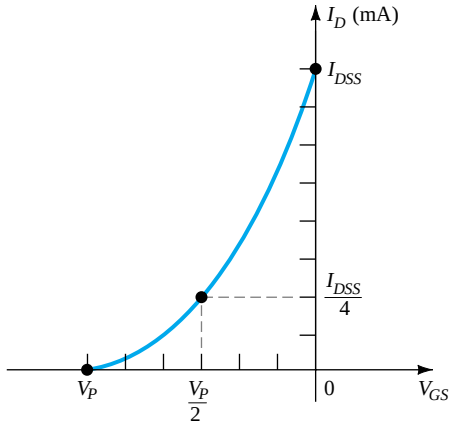


Figure .3 Plotting Shockley'

In Fig..4,the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves

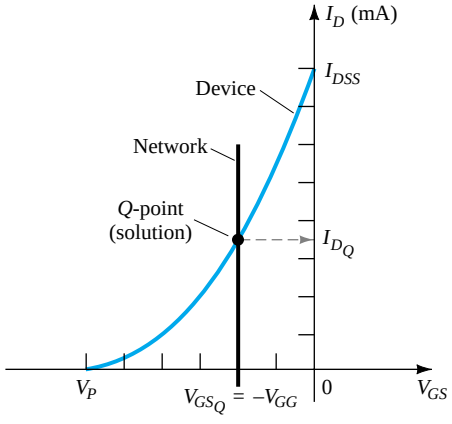


Figure 4 Finding the solution for the fixed-bias configuration.

intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.* The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 6.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis as shown in Fig. 4. It is important to realize that once the net-work of Fig. 1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 5 are the quiescent values defined by Fig.4.

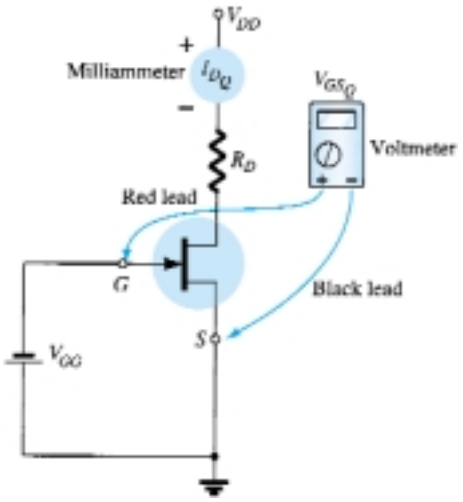


Figure .5 Measuring the qui-escent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{6}$$

Recall that single-subscript voltages refer to the voltage at a point with ground. For the configuration of Fig. 6.2,

$$\boxed{V_S = 0 \text{ V}} \quad \text{(respect to)} \tag{7}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

and

$$\boxed{V_D = V_{DS}} \tag{8}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

and

$$\boxed{V_G = V_{GS}} \tag{9}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE .1

Determine the following for the network of Fig..6.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.

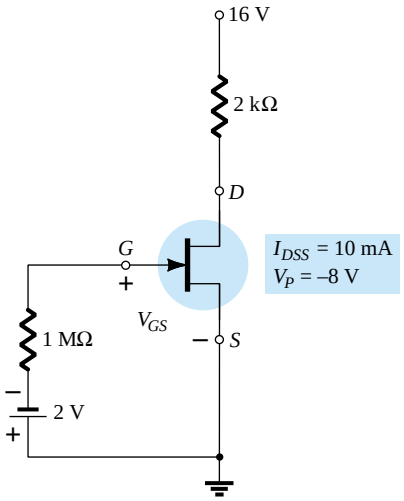


Figure.6

Solution

Mathematical Approach:

(a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$

(b) $I_{DQ} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \dfrac{-2\text{ V}}{-8\text{ V}}\right)^2$

$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$

$= \mathbf{5.625\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$

$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Graphical Approach:

The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7. It is certainly difficult to read beyond the second place without significantly in-

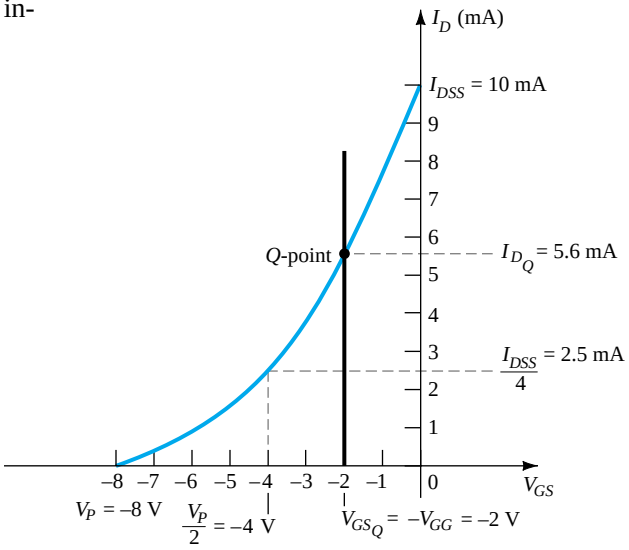


Figure 7 Graphical solution for the network

creasing the size of the figure, but a solution of 5.6 mA from the graph of Fig..7 is quite acceptable. Therefore, for part (a),

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

II. SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 6.8.

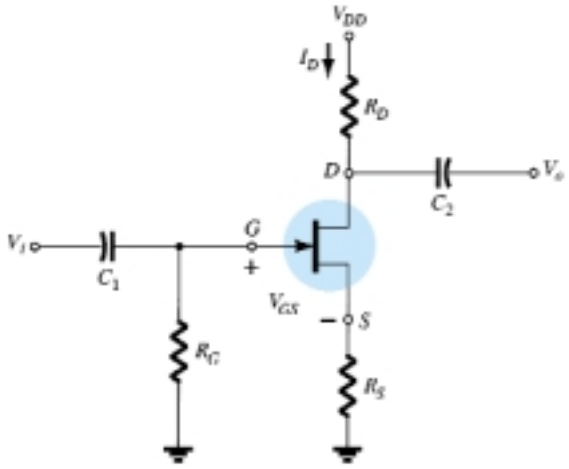


Figure 8 JFET self-bias con-figuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 6.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_s} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_s} = 0$$

and

$$V_{GS} = -V_{R_s}$$

or

$$\boxed{V_{GS} = -I_D R_S} \qquad (10)$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in nitude as occurred for the fixed-bias configuration.
mag-

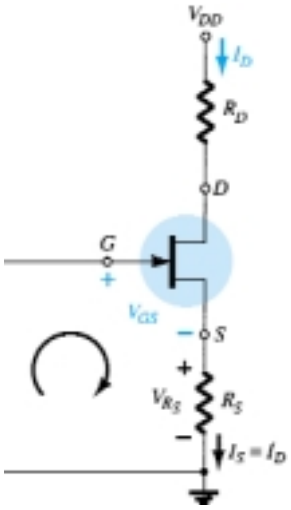


Figure 9 DC analysis of the self-bias configuration.

Equation (10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, permitting either a mathematical or graphical solution.

A mathematical solution could be obtained simply by substituting Eq. (10) into Shockley's equation as shown below:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 10. Since Eq. (10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points.

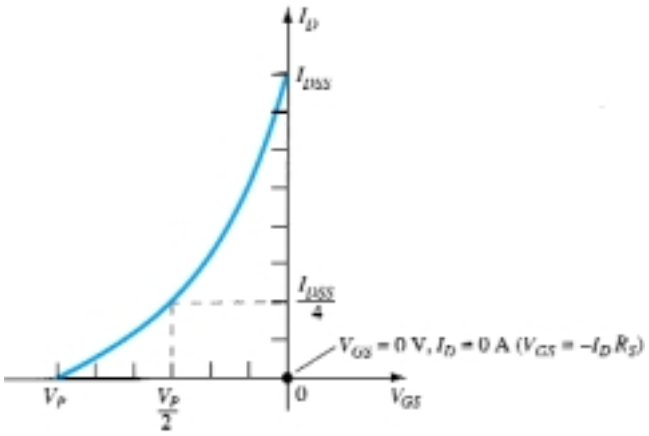


Figure 10 Defining a point on the self-bias line.

The second point for Eq. (10) requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined using Eq. (10). The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit an actual drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

then

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. .11. The straight line as defined by Eq. (10) is then drawn and the quiescent point obtained at the in-

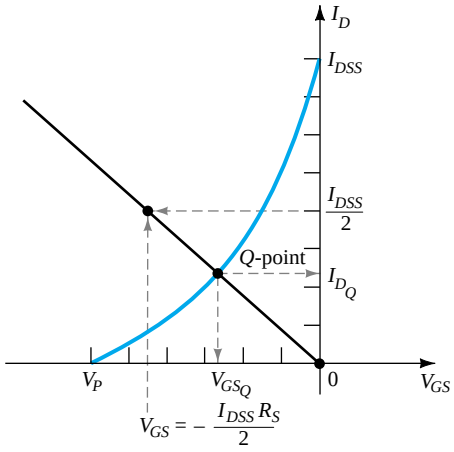


Figure .11 Sketching the self-bias line.

tersection of the straight-line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and
$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but
$$I_D = I_S$$

and
$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{11}$$

In addition:

$$\boxed{V_S = I_D R_S} \tag{12}$$

$$\boxed{V_G = 0\ \text{V}} \tag{13}$$

and
$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \tag{14}$$

EXAMPLE 2

Determine the following for the network of Fig. 12.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.

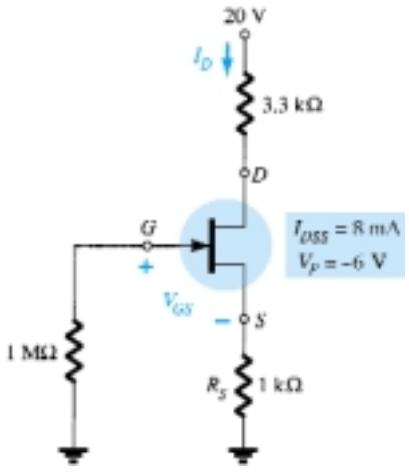


Figure 12

Solution

(a) The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

The result is the plot of Fig. 6.13 as defined by the network.

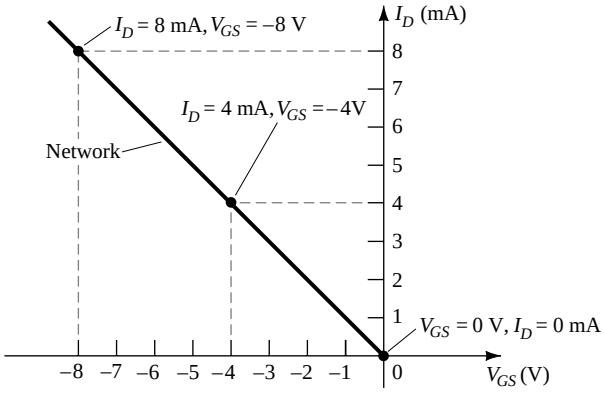


Figure 13 Sketching the self-bias line for the network of Fig. 6.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D calculated with the same resulting plot.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8$ mA$/4 = 2$ mA, and the plot of Fig. 14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 13 on the device characteristics of Fig. 6.14 and finding the point of intersection of the two as indicated on Fig. 15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6 \text{ V}}$$

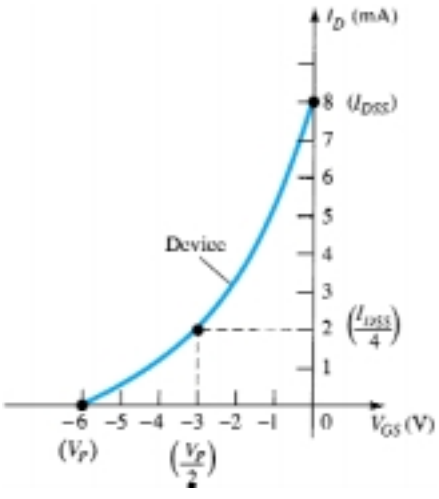


Figure 14 Sketching the device characteristics for the JFET of Fig. 6.12.

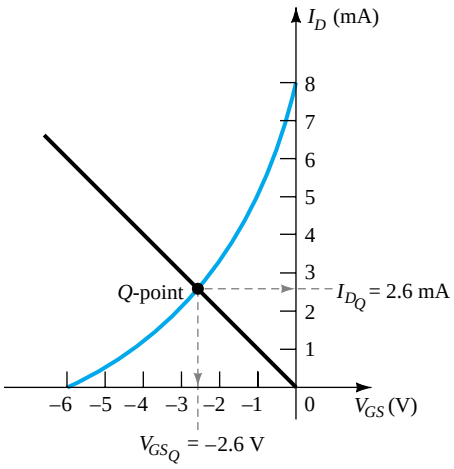


Figure 15 Determining the *Q*-point for the network of Fig. 6.12.

(b) At the quiescent point:

$$I_{DQ} = \mathbf{2.6\ mA}$$

(c) Eq. (6.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$
$= 20\ \text{V} - 11.18\ \text{V}$
$= \mathbf{8.82\ V}$

(d) Eq. (6.12): $V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

(e) Eq. (6.13): $V_G = \mathbf{0\ V}$

(f) Eq. (6.14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

EXAMPLE .3

Find the quiescent point for the network of Fig..12 if:
(a) $R_S = 100\ \Omega$.
(b) $R_S = 10\ \text{k}\Omega$.

Solution

Note Fig. 6.16.

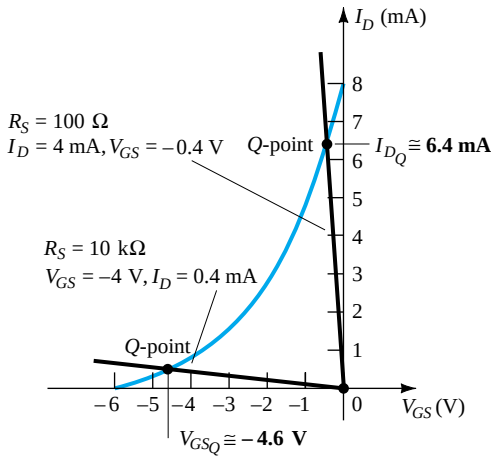


Figure.16

(a) With the I_D scale,

$$I_{DQ} \cong \mathbf{6.4\ mA}$$

From Eq. (6.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

(b) With the V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

From Eq. (6.10),

$$I_{DQ} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis while increasing levels of R_S bring the load line closer to the V_{GS} axis.

EXAMPLE 4

Determine the following for the common-gate configuration of Fig. 17.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_D.
(d) V_G.
(e) V_S.
(f) V_{DS}.

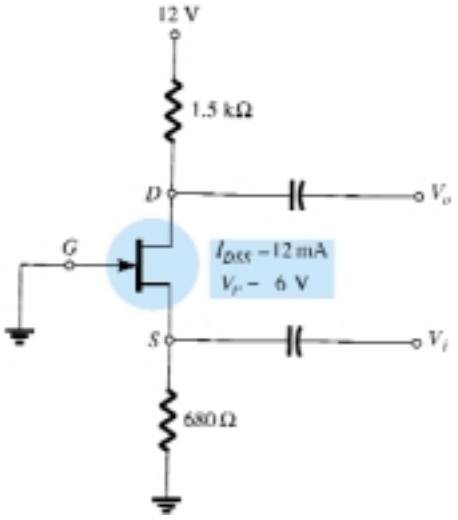


Figure .17

Solution

The grounded gate terminal and the location of the input establish strong similarities with the common-base BJT amplifier. Although different in appearance from the ba-sic structure of Fig..8, the resulting dc network of Fig. 18 has the same basic struc-ture as Fig. .9. The dc analysis can therefore proceed in the same manner as recent examples.

(a) The transfer characteristics and load line appear in Fig. 19. In this case, the second point for the sketch of the load line was determined by choosing (arbitrarily) $I_D = 6$ mA and solving for V_{GS}. That is,

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 6.19. The device transfer curve was sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}$$

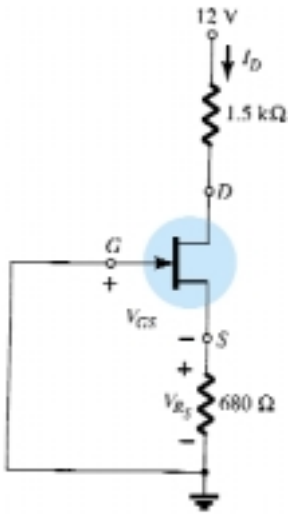


Figure 18 Sketching the dc equivalent of the network of Fig. 6.17.

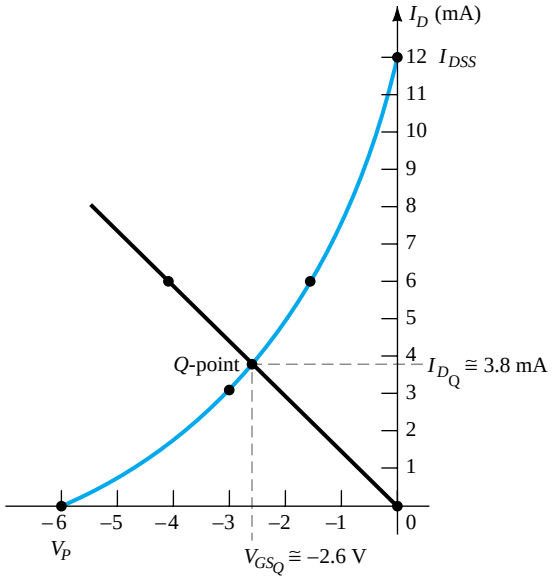


Figure 19 Determining the *Q*-point for the network of Fig. 6.17.

and the associated value of V_{GS}:

$$V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

as shown on Fig. 6.19. Using the resulting quiescent point of Fig. 6.19 results in

$$V_{GSQ} \cong \mathbf{-2.6\text{ V}}$$

(b) From Fig. 6.19,

$$I_{DQ} \cong \mathbf{3.8\text{ mA}}$$

(c) $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\text{ V}}$

(d) $V_G = \mathbf{0\text{ V}}$

(e) $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$
$= \mathbf{2.58\text{ V}}$

(f) $V_{DS} = V_D - V_S$
$= 6.3\text{ V} - 2.58\text{ V}$
$= \mathbf{3.72\text{ V}}$

III VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig.20. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network of Fig. 20 is redrawn as shown in Fig. 21 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equiv-

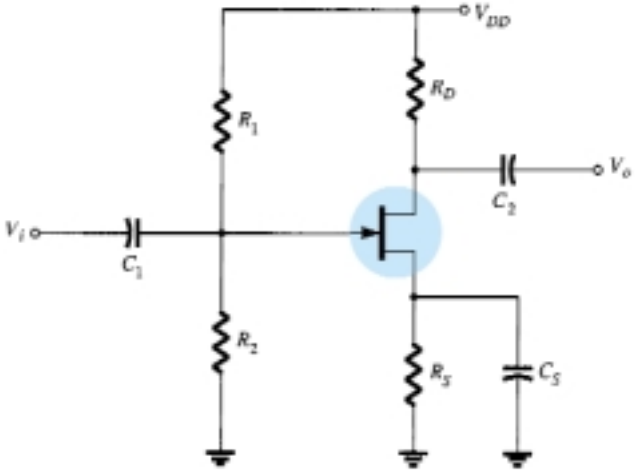


Figure 20 Voltage-divider bias arrangement.

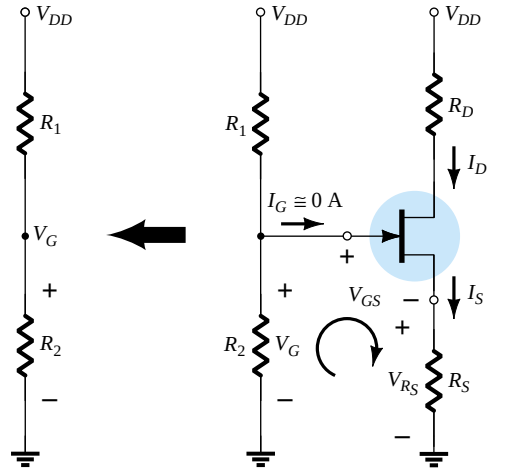


Figure.21 Redrawn network of Fig. 6.20 for dc analysis.

alent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{15}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 6.21 will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_s} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \tag{16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that *anywhere on the horizontal axis* of Fig. 22 the current $I_D = 0$ mA. If we therefore *select* I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (16) and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0 \text{ mA}) R_S$$

and

$$V_{GS} = V_G\big|_{I_D = 0 \text{ mA}} \tag{17}$$

The result specifies that whenever we plot Eq. (16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 22.

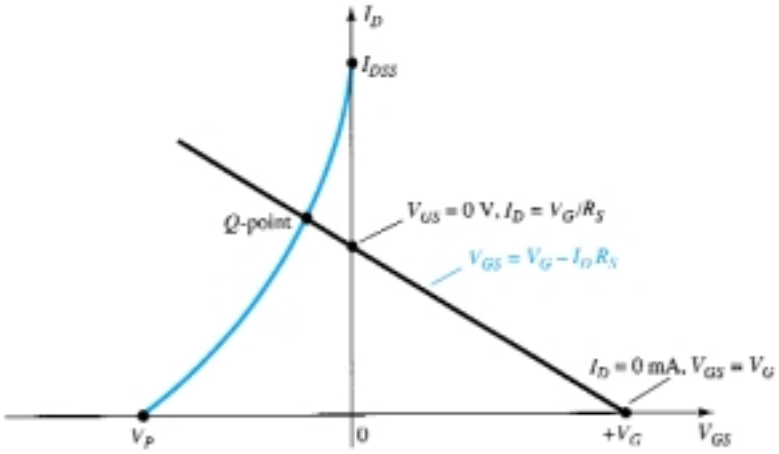


Figure 22 Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$

$$0 \text{ V} = V_G - I_D R_S$$

and

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0 \text{ V}}} \tag{18}$$

The result specifies that whenever we plot Eq. (66), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (18). This intersection also appears on Fig. 22.

The two points defined above permit the drawing of a straight line to represent Eq. (16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as shown in Fig. 6.23. It is fairly obvious from Fig..23 that:

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

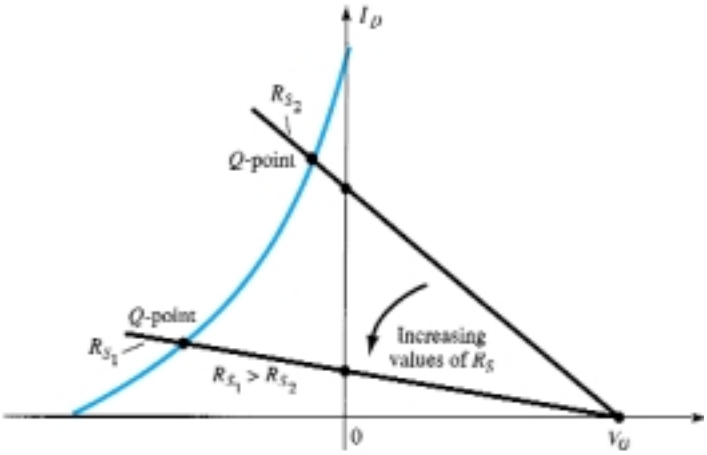


Figure 23 Effect of R_S on the resulting Q-point.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \tag{19}$$

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{20}$$

$$\boxed{V_S = I_D R_S} \tag{21}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}} \quad 22)$$

EXAMPLE 5

Determine the following for the network of Fig..24.

(a) I_{DQ} and V_{GSQ}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.

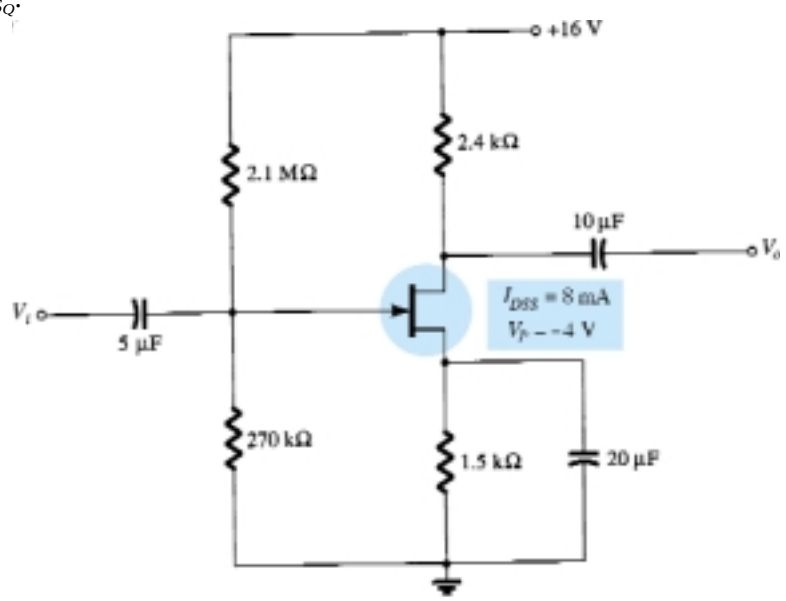


Figure .24

Solution

(a) For the transfer characteristics, if $I_D = I_{DSS}/4 = 8$ mA/4 = 2 mA, then $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$. The resulting curve representing Shockley's equation ap-pears in Fig. 25. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$

$$= 1.82\ \text{V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\ \text{V}$$

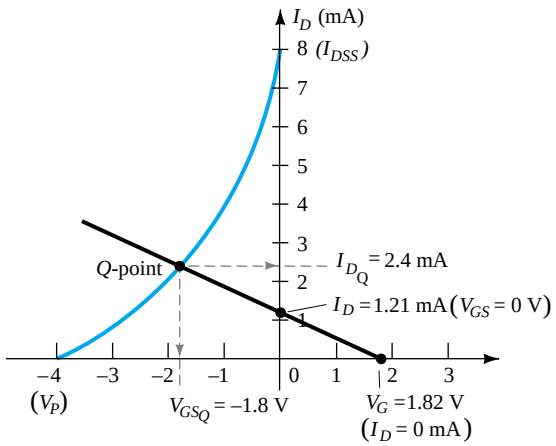


Figure.25 Determining the *Q*-point for the network .

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 6.25 with quiescent values of

$$I_{D_Q} = \mathbf{2.4 \text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8 \text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$
$= \mathbf{10.24 \text{ V}}$

(c) $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$
$= \mathbf{3.6 \text{ V}}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$
$= \mathbf{6.64 \text{ V}}$
or $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$
$= \mathbf{6.64 \text{ V}}$

(e) Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24 \text{ V} - 1.82 \text{ V}$$
$$= \mathbf{8.42 \text{ V}}$$

Although the basic construction of the network in the next example is quite different from the voltage-divider bias arrangement, the resulting equations require a solution very similar to that just described. Note that the network employs a supply at the drain and source.

EXAMPLE .6

Determine the following for the network of Fig. 26.
(a) I_{DQ} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.
(d) V_S.

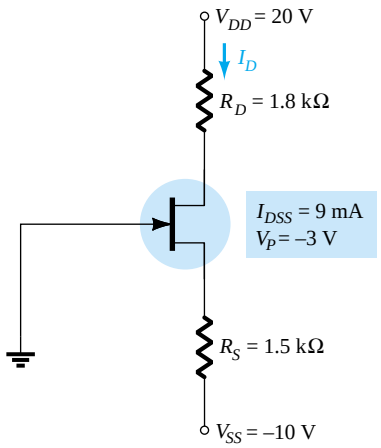


Figure 26

Solution

(a) An equation for V_{GS} in terms of I_D is obtained by applying Kirchhoff's voltage law to the input section of the network as redrawn in Fig. 27.

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or
$$V_{GS} = V_{SS} - I_S R_S$$

but
$$I_S = I_D$$

and
$$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad (23)$$

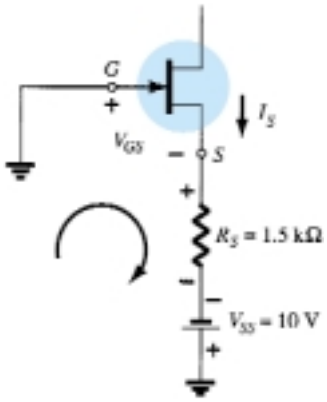


Figure 27 Determining the network equation for the configu-ration of Fig. 26.

$$V_{GS} = 10\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

For $I_D = 0$ mA,

$$V_{GS} = V_{SS} = 10\ \text{V}$$

For $V_{GS} = 0$ V,

$$0 = 10\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

and
$$I_D = \frac{10\ \text{V}}{1.5\ \text{k}\Omega} = 6.67\ \text{mA}$$

The resulting plot points are identified on Fig. 6.28.

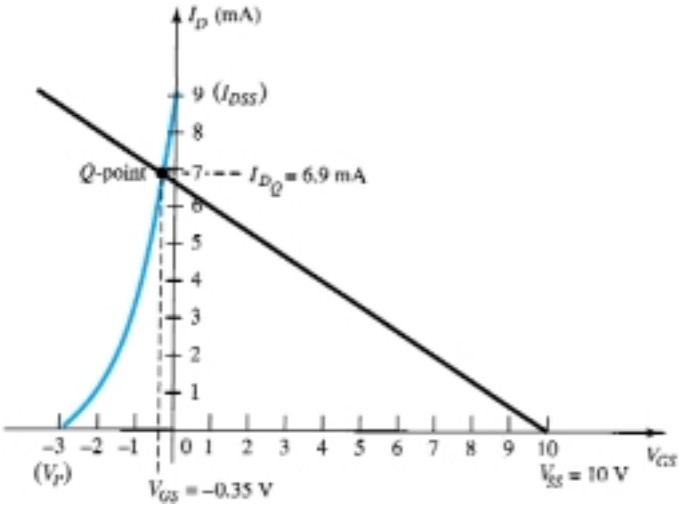


Figure 28 Determining the *Q*-point for the network

The transfer characteristics are sketched using the plot point established by $V_{GS} = V_P/2 = -3\ \text{V}/2 = -1.5\ \text{V}$ and $I_D = I_{DSS}/4 = 9\ \text{mA}/4 = 2.25\ \text{mA}$, as also appearing on Fig. 28. The resulting operating point establishes the following quiescent levels:

$$I_{D_Q} = \mathbf{6.9\ mA}$$

$$V_{GS_Q} = \mathbf{-0.35\ V}$$

(b) Applying Kirchhoff's voltage law to the output side of Fig. 26 will result in

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S) \tag{24}$$

which for this example results in

$$V_{DS} = 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= 30\text{ V} - 22.77\text{ V}$$
$$= \mathbf{7.23\text{ V}}$$

(c) $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$
$= \mathbf{7.58\text{ V}}$

(d) $V_{DS} = V_D - V_S$
or $V_S = V_D - V_{DS}$
$= 7.58\text{ V} - 7.23\text{ V}$
$= \mathbf{0.35\text{ V}}$

IV. DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the impact of the change in device on the resulting analysis.

EXAMPLE 7

For the *n*-channel depletion-type MOSFET of Fig. 6.29, determine:
(a) I_{DQ} and V_{GSQ}.
(b) V_{DS}.

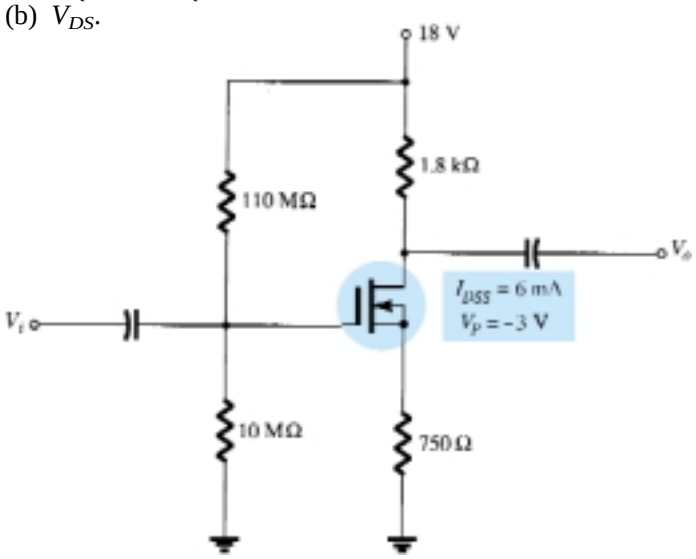


Figure 29 Example 7.

Solution

(a) For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 6.30. Proceeding as described for JFETs, we have:

$$\text{Eq. (6.15):} \quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (6.16):} \quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

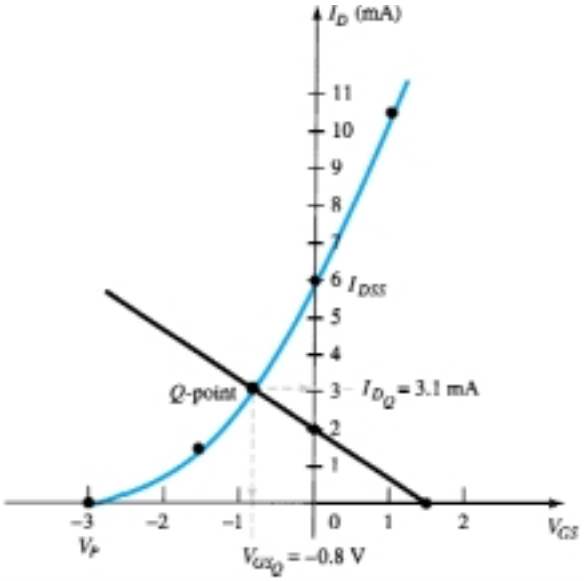


Figure 30

Setting $I_D = 0\text{ mA}$ results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0\text{ V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 6.30. The resulting operating point:

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$

$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

(b) Eq. (6.19): $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$

$\cong \mathbf{10.1\text{ V}}$

EXAMPLE 8 Repeat Example 7 with $R_S = 150\ \Omega$.

Solution

(a) The plot points are the same for the transfer curve as shown in Fig. 31. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

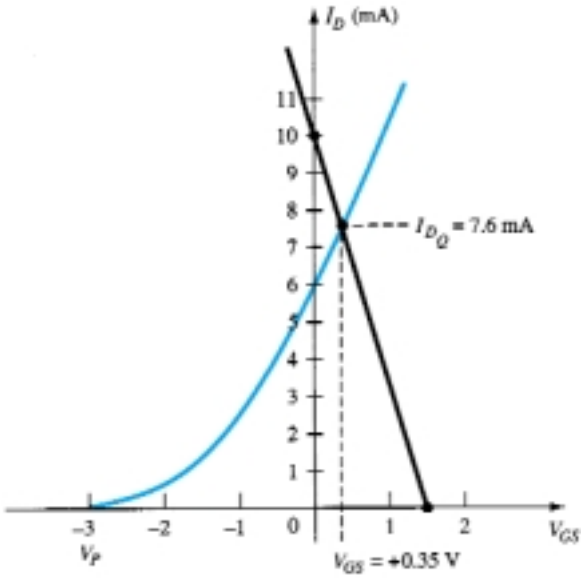


Figure 31

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$

The bias line is included on Fig. 6.31. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result:

$$I_{DQ} = \mathbf{7.6\text{ mA}}$$

$$V_{GSQ} = \mathbf{+0.35}$$

V(b) Eq. (19): $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega)$

$= \mathbf{3.18\text{ V}}$

EXAMPLE 9

Determine the following for the network of Fig. 32.

(a) I_{DQ} and V_{GSQ}.
(b) V_D.

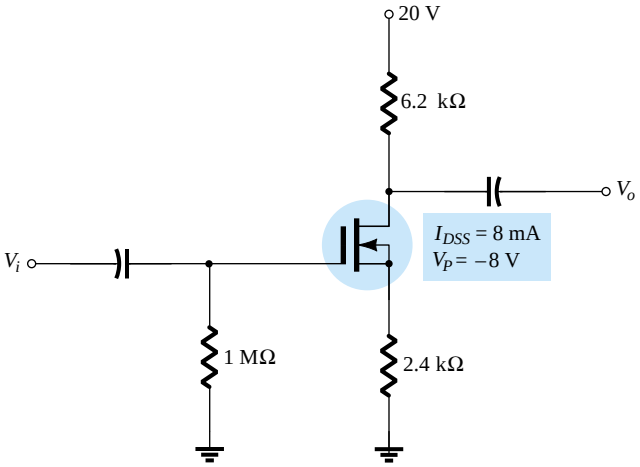


Figure 32

Solution

(a) The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than zero volts. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2 \text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8 \text{ mA}\left(1 - \frac{+2 \text{ V}}{-8 \text{ V}}\right)^2$$

$$= 12.5 \text{ mA}$$

The resulting transfer curve appears in Fig. 6.33. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6 \text{ V}}{2.4 \text{ k}\Omega} = 2.5 \text{ mA}$$

The resulting Q-point:

$$I_{D_Q} = \mathbf{1.7 \text{ mA}}$$

$$V_{GSQ} = \mathbf{-4.3 \text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$

$= 20 \text{ V} - (1.7 \text{ mA})(6.2 \text{ k}\Omega)$

$= \mathbf{9.46 \text{ V}}$

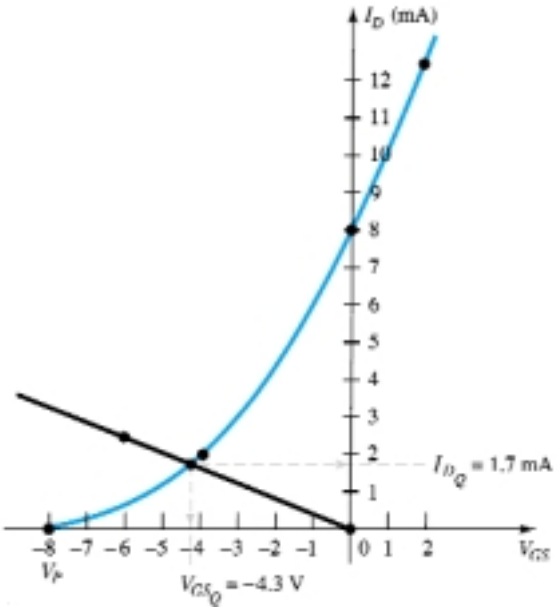


Figure 33 Determining the *Q*-point for the network of Fig. 32.

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

EXAMPLE 10

Determine V_{DS} for the network of Fig. 34.

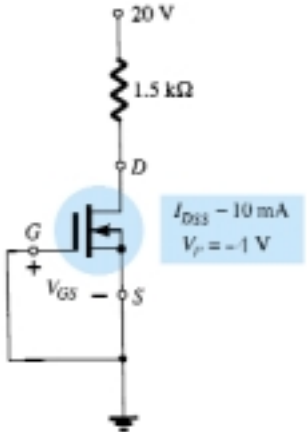


Figure 34 Example.10.

Solution

The direct connection between the gate and source terminals requires that

$$V_{GS} = 0 \text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0\ V}$$

and

$$I_{D_Q} = \mathbf{10\ mA}$$

There is therefore no need to draw the transfer curve and

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega)$$
$$= 20 \text{ V} - 15 \text{ V}$$
$$= \mathbf{5\ V}$$

V. ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 35. For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

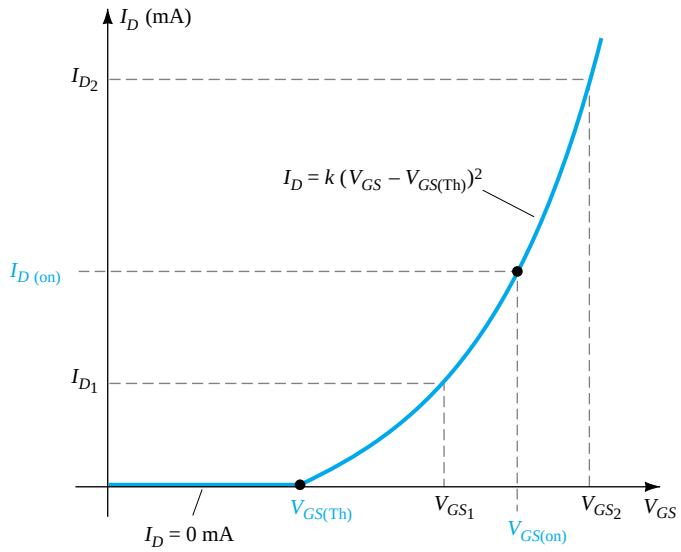


Figure 6.35 Transfer characteristics of an *n*-channel enhancement-type MOSFET.

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \tag{25}$$

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(on)}$) and its corresponding level of $V_{GS(on)}$, two points are defined immediately as shown in Fig. 35. To complete the curve, the constant k of Eq. (25) must be determined from the specification sheet data by substituting into Eq. (25) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$

$$I_{D(on)} = k(V_{GS(on)} - V_{GS(Th)})^2$$

and

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2} \tag{26}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}.

Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 36. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA and $V_{RG} = 0$ V, the dc equivalent network appears as shown in Fig. 37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS} \tag{27}$$

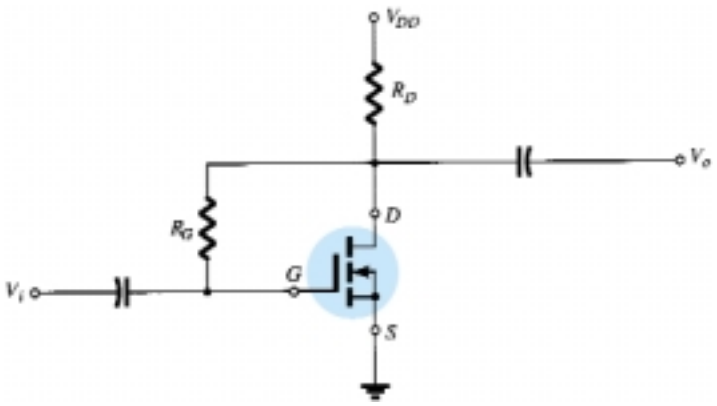


Figure 36 Feedback biasing arrangement.

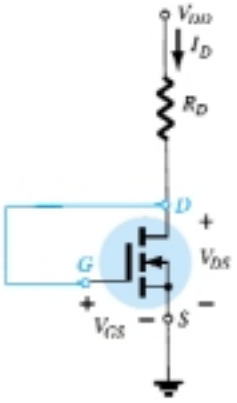


Figure 37 DC equivalent of the network of Fig. 36.

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (6.27):

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \tag{28}$$

The result is an equation that relates the same two variables as Eq. (25), permitting the plot of each on the same set of axes.

Since Eq. (28) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Sub-stituting $I_D = 0$ mA into Eq. (28) gives

$$\boxed{V_{GS} = V_{DD}\big|_{I_D\,=\,0\text{ mA}}} \tag{29}$$

Substituting $V_{GS} = 0$ V into Eq. (6.28), we have

$$\boxed{I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS}\,=\,0\text{ V}}} \tag{30}$$

The plots defined by Eqs. (25) and (28) appear in Fig. 38 with the resulting operating point.

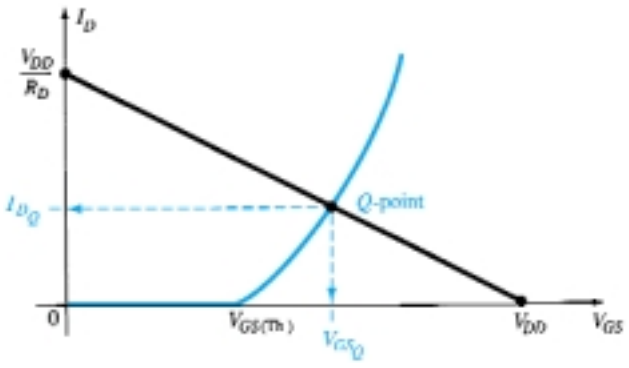


Figure 38 Determining the *Q*-point for the network of Fig. 36.

Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 39. *EXAMPLE .11*

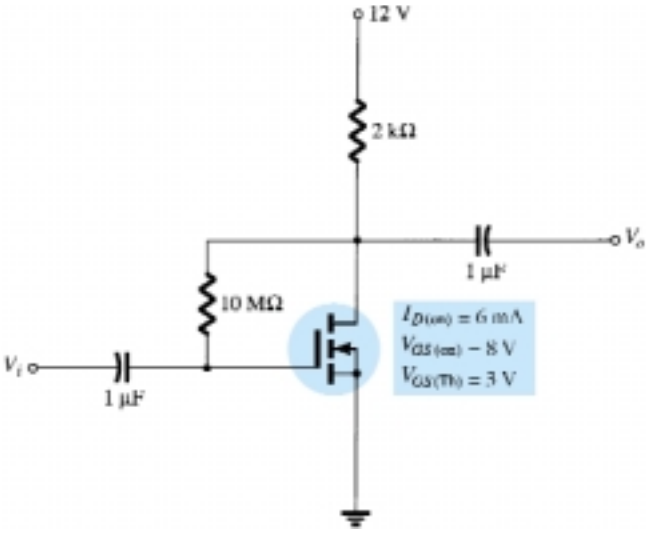


Figure 39 Example .11.

Solution

Plotting the Transfer Curve:

Two points are defined immediately as shown in Fig. 6.40. Solving for k:

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{A/v}^2$$

$$= \mathbf{0.24 \times 10^{-3} \text{ A/V}^2}$$

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16 \text{ mA}$$

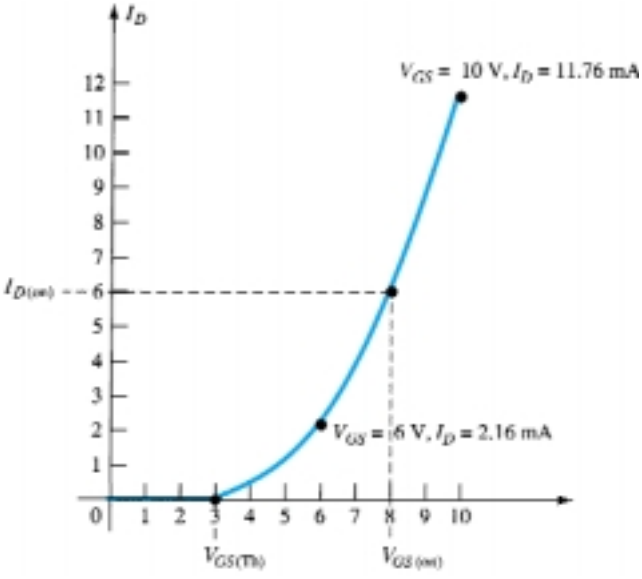


Figure 40 Plotting the transfer curve for the MOSFET of Fig. 39.

as shown on Fig. 6.40. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$):

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

as also appearing on Fig. 6.40. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 6.40.

For the Network Bias Line:

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

Eq. (6.29): $V_{GS} = V_{DD} = 12\text{ V}\big|_{I_D = 0\text{ mA}}$

Eq. (6.30): $I_D = \dfrac{V_{DD}}{R_D} = \dfrac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}\big|_{V_{GS} = 0\text{ V}}$

The resulting bias line appears in Fig. 6.41.

At the operating point:

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

and $$V_{GS_Q} = 6.4\text{ V}$$

with $$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

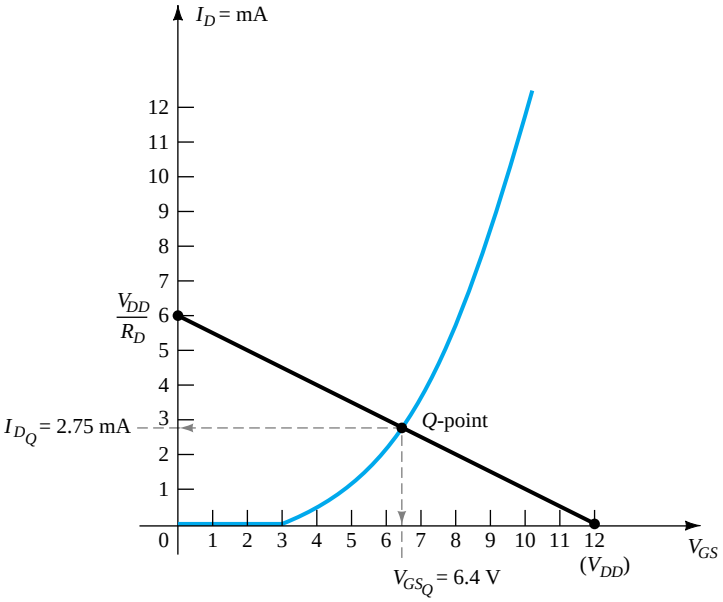


Figure 41 Determining the *Q*-point for the network of Fig. 6.39.

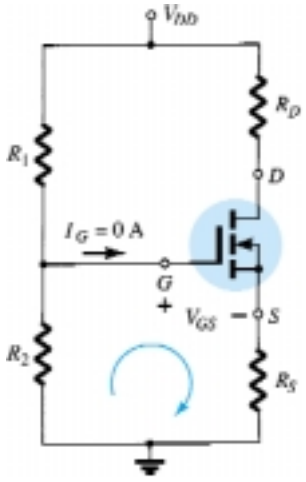


Figure 42 Voltage-divider biasing arrangement for an *n*-channel enhancement MOSFET.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 6.42. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{31}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 42 will result in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S} \qquad (32)$$

For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \qquad (33)$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (6.32) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 12

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig.43.

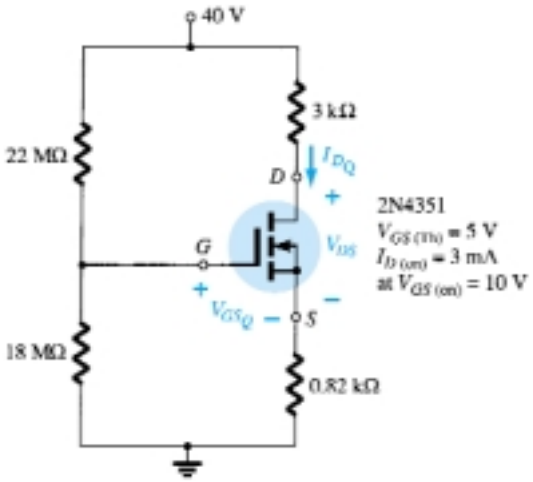


Figure 43 Example.12.

Solution

Network:

$$\text{Eq. (6.31):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$\text{Eq. (6.32):} \quad V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

as appearing on Fig. 6.44. When $V_{GS} = 0$ V,

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$

as appearing on Fig. 44.

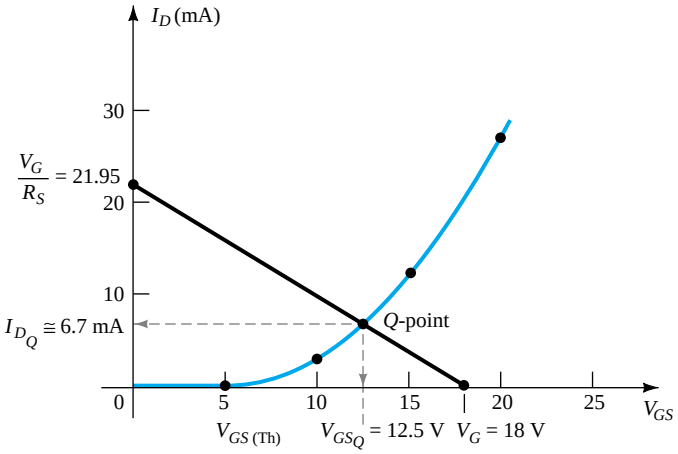


Figure 44 Determining the *Q*-point for the network of Example 12.

Device:

$$V_{GS(\text{Th})} = 5\text{ V}, \qquad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 6.44). From Fig. 6.44,

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

$$\text{Eq. (6.33):} \quad V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega)$$

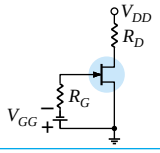
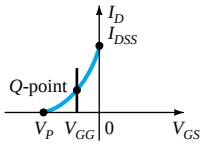
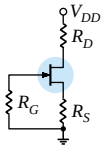
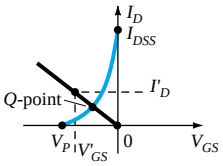
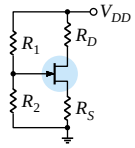
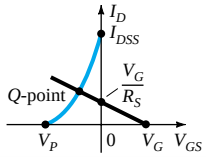
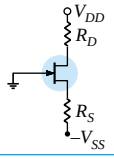
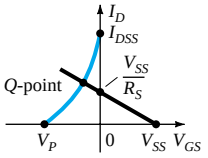
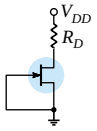
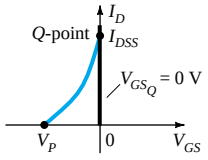
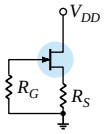
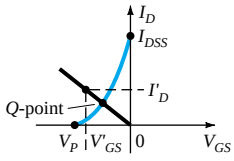
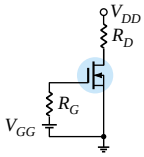
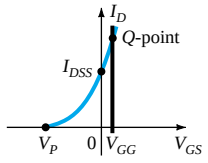
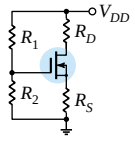
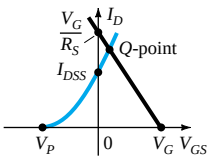
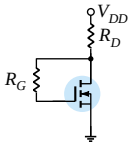
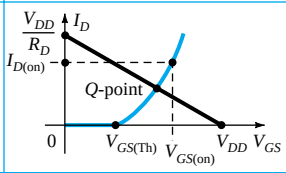
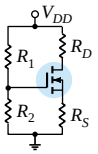
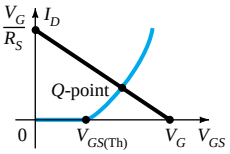
$$= 40\text{ V} - 25.6\text{ V}$$

$$= \mathbf{14.4\text{ V}}$$

6.7 SUMMARY TABLE

Now that the most popular biasing arrangements for the various FETs have been introduced, Table 6.1 reviews the basic results and demonstrates the similarity in approach for a number of configurations. It also reveals that the general analysis of dc configurations for FETs is not overly complex. Once the transfer characteristics are established, the network self-bias line can be drawn and the *Q*-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

TABLE 6.1 FET Bias Configurations

Type	*Configuration*	*Pertinent Equations*	*Graphical Solution*
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GSQ} = 0$ V)		$V_{GSQ} = 0$ V $I_{DQ} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement- type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

I. FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

Recall from Chapter 6 that a dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \, \Delta V_{GS} \tag{1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and input quantity. The root word *conductance* was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$.

Solving for g_m in Eq. (1), we have:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 9.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \tag{3}$$

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. Or, in other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

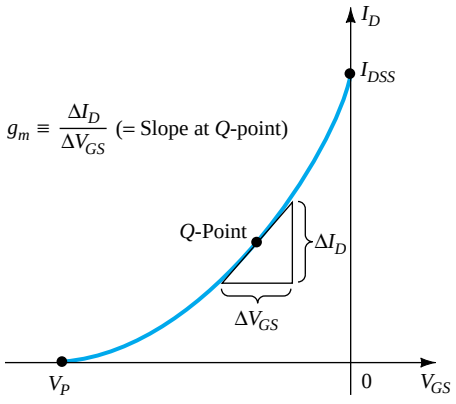


Figure .1 Definition of g_m using transfer characteristic.

Equation (2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (2) to determine g_m.

EXAMPLE .1

Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points:
(a) $V_{GS} = -0.5$ V.
(b) $V_{GS} = -1.5$ V.
(c) $V_{GS} = -2.5$ V.

Solution

The transfer characteristics are generated as Fig. 2 using the procedure defined in Chapter 6. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate in-crement is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (9.2) is then applied to determine g_m.

(a) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$$

(b) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$$

(c) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$$

Note the decrease in g_m as V_{GS} approaches V_P.

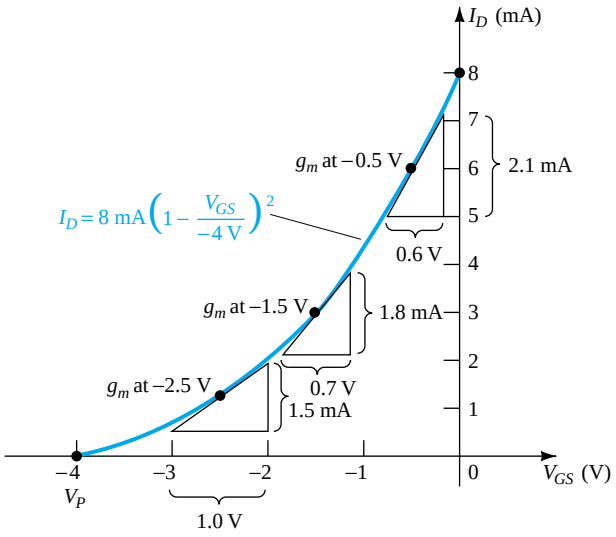


Figure 2 Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph the better the accuracy, but this can then become a cumbersome

problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, an equation for g_m can be derived as follows:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{Q\text{-pt.}} = \frac{dI_D}{dV_{GS}}\bigg|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{4}$$

where $|V_P|$ denotes magnitude only to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (4) will result in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (9.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{6}$$

EXAMPLE.2

For the JFET having the transfer characteristics of Example 1:
(a) Find the maximum value of g_m.
(b) Find the value of g_m at each operating point of Example 9.1 using Eq. (6) and compare with the graphical results.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\ mS}$ (maximum possible value of g_m)

(b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\ mS}$$ (versus 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\ mS} \quad \text{(versus 2.57 mS graphically)}$$

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\ mS} \quad \text{(versus 1.5 mS graphically)}$$

The results of Example 9.2 are certainly sufficiently close to validate Eq. (4) through (6) for future use when g_m is required.

On specification sheets, g_m is provided as y_{fs} where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer parameter, and the s reveals that it is connected to the source terminal.

In equation form,

$$g_m = y_{fs} \tag{7}$$

Plotting g_m vs. V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (9.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (9.6) defines a straight line with a minimum value of 0 and a maximum value of g_m as shown by the plot of Fig. 9.3.

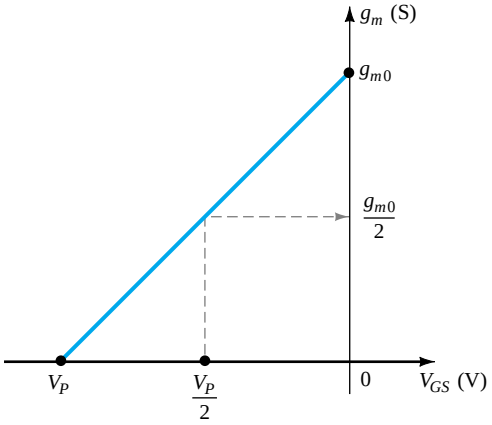


Figure 3 Plot of g_m vs. V_{GS}.

Figure 9.3 also reveals that when V_{GS} is one-half the pinch-off value, g_m will be one-half the maximum value.

EXAMPLE 3

Plot g_m vs. V_{GS} for the JFET of examples 1 and 2.

Solution

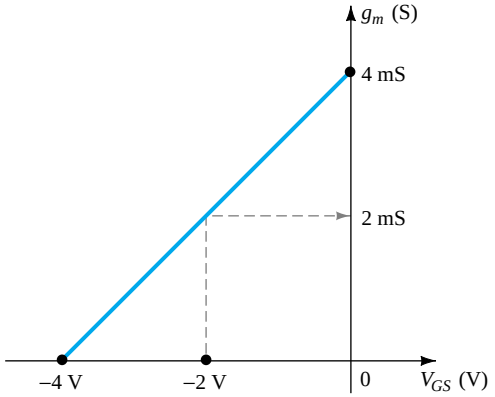


Figure 4 Plot of g_m vs. V_{GS} for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V.

Impact of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \tag{.8}$$

Substituting Eq. (9.8) into Eq. (9.6) will result in

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \tag{9}$$

Using Eq. (9.9) to determine g_m for a few specific values of I_D, the results are

(a) If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \boldsymbol{g_{m0}}$$

(b) If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707}\boldsymbol{g_{m0}}$$

(c) If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5}\boldsymbol{g_{m0}}$$

EXAMPLE .4 Plot g_m vs. I_D for the JFET of Examples 1 through 3.

Solution

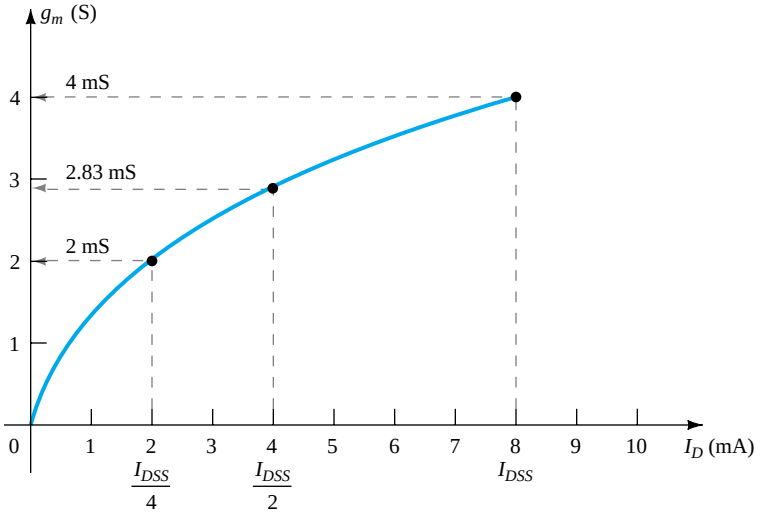


Figure .5 Plot of g_m vs. I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of Examples 9.3 and 9.4 clearly reveal that the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D its maximum value of I_{DSS}.

FET Input Impedance Z_i

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i \text{ (FET)} = \infty \tag{10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, while a value of $10^{15}\ \Omega$ is typical for MOSFETs.

FET Output Impedance Z_o

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (source) to which it is attached in the model. For the JFET of Fig. 5.18, y_{os} has a range of 10 to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o \text{ (FET)} = r_d = \frac{1}{y_{os}} \tag{11}$$

The output impedance is defined on the characteristics of Fig. 9.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater the output impedance. If perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{12}$$

g_m

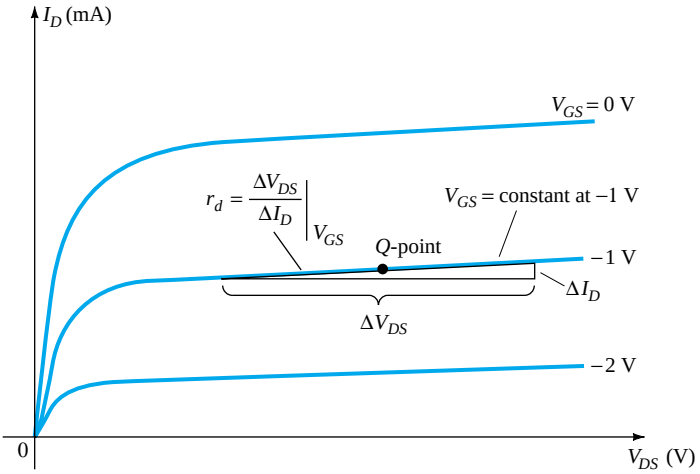


Figure .6 Definition of r_d using FET drain characteristics.

EXAMPLE 5

Determine the output impedance for the FET of Fig..7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

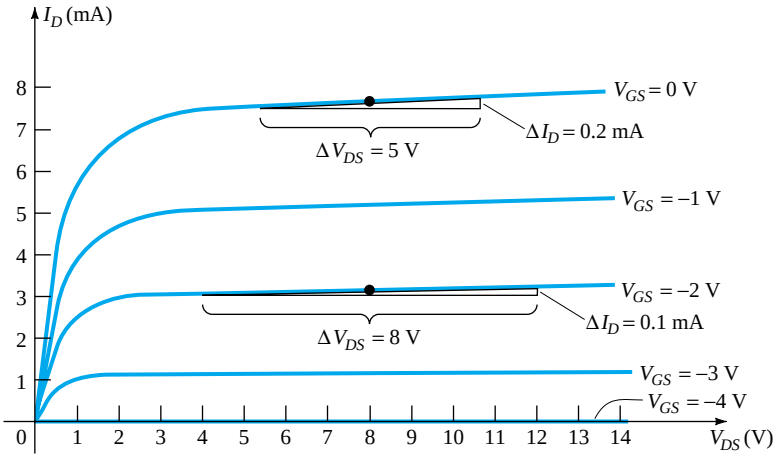


Figure 7 Drain characteristics used to calculate r_d in Example.5.

Solution

For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (12),

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (12),

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$

revealing that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

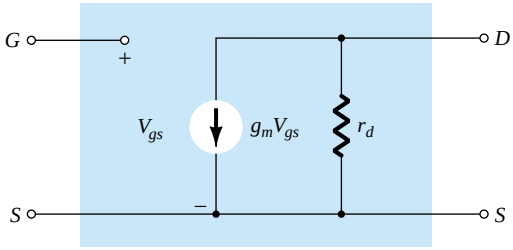


Figure.8 FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate to source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled device.

EXAMPLE.6

Given $y_{fs} = 3.8$ mS and $y_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution

$$g_m = y_{fs} = 3.8\text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 9.9.

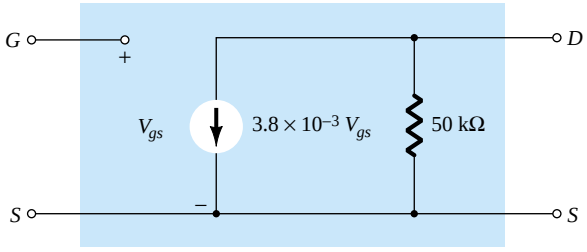


Figure 9 FET ac equivalent model for Example 6.

g_m

II. JFET FIXED-BIAS CONFIGURATION

Now that the FET equivalent circuit has been defined, a number of fundamental FET small-signal configurations will be investigated. The approach will parallel the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 9.10 includes the coupling capacitors C_1 and C_2 that isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

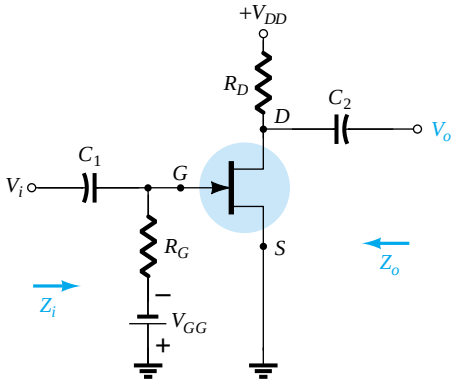


Figure 10 JFET fixed-bias configuration.

Once the level of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 9.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to zero volts by a short-circuit equivalent.

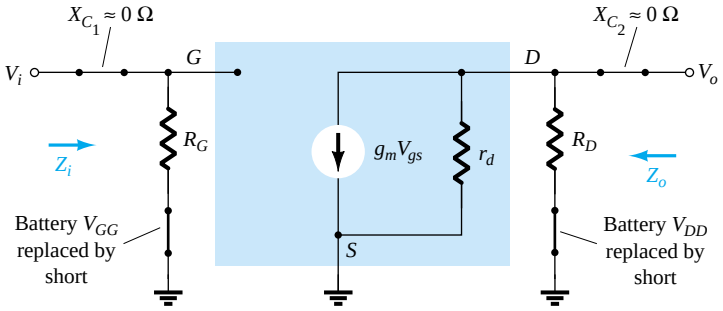


Figure .11 Substituting the JFET ac equivalent circuit unit into the network of Fig. 9.10.

The network of Fig. is then carefully redrawn as shown in Fig. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across R_D by V_o.

***Zi*:** Figure 12 clearly reveals that

$$Z_i = R_G \tag{13}$$

because of the open-circuit equivalence at the input terminals of the JFET.

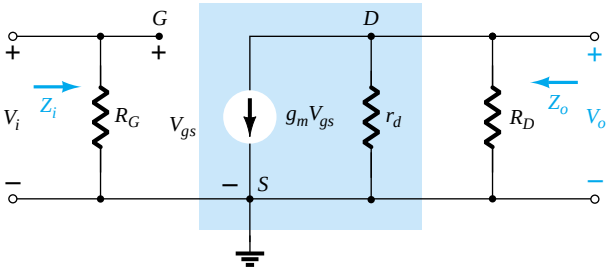


Figure.12 Redrawn network of Fig. .11.

***Z*$_o$:** Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 13. The output impedance is

$$Z_o = R_D \| r_d \tag{14}$$

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{15}$$

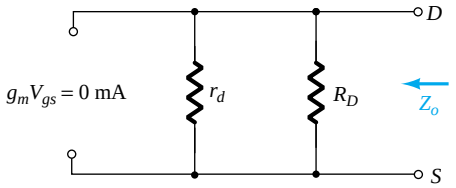


Figure .13 Determining Z_o.

***A*$_v$:** Solving for V_o in Fig. 12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{16}$$

If $r_d \geq 10R_D$:

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D \tag{17}$$

Phase Relationship: The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE .7

The fixed-bias configuration of Example 1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 4 with an applied signal V_i. The value of y_{os} is provided as 40 μS. (a) Determine g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o.
(e) Determine the voltage gain A_v.
(f) Determine A_v ignoring the effects of r_d.

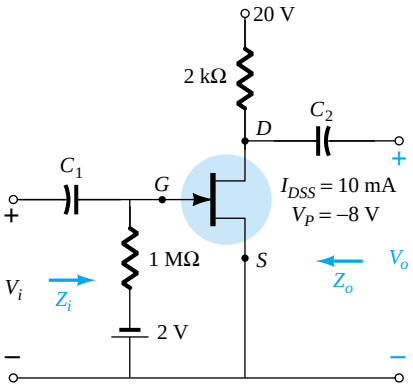


Figure 14 JFET configuration for Example .7.

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\ mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D resulted in a difference of 8% in solution.

III. JFET SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 15 requires only one dc supply to establish the desired operating point.

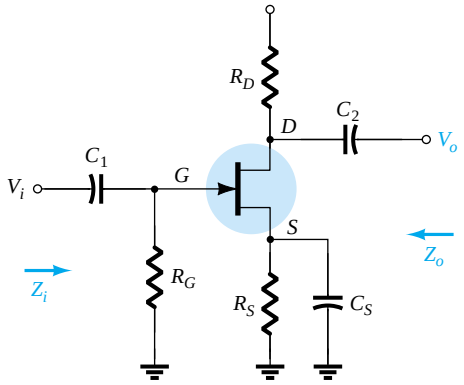


Figure 15 Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its short-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 16 and carefully redrawn in Fig. 17.

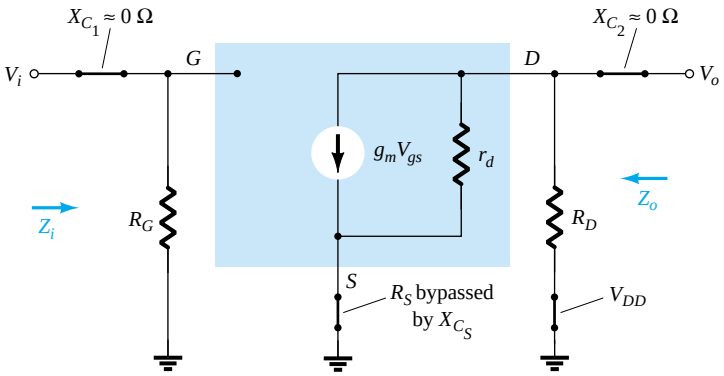


Figure 16 Network of Fig. 9.15 following the substitution of the JFET ac equivalent circuit.

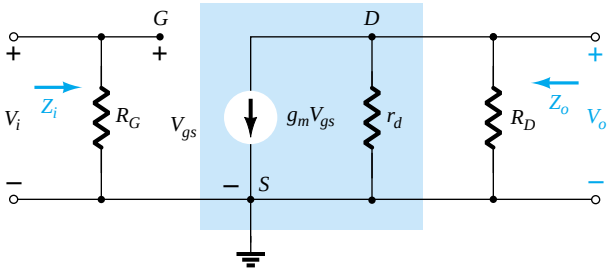


Figure 17 Redrawn network of Fig..16.

Since the resulting configuration is the same as appearing in Fig. 9.12, the resulting equations Z_i, Z_o, and A_v will be the same.

***Zi*:**

$$Z_i = R_G \tag{18}$$

g_m

Z_o:

$$Z_o = r_d \| R_D \tag{19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D} \tag{20}$$

A_v:

$$A_v = -g_m(r_d \| R_D) \tag{21}$$

If $r_d \ 10R_D$,

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D} \tag{22}$$

Phase relationship: The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 15, the resistor R_S will be part of the ac equivalent cir- cuit as shown in Fig..18. In this case, there is no obvious way to reduce the net- work to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must simply be very careful with notation and defined polarities and direction. Ini- tially, the resistance r_d will be left out of the analysis to form a basis for comparison.

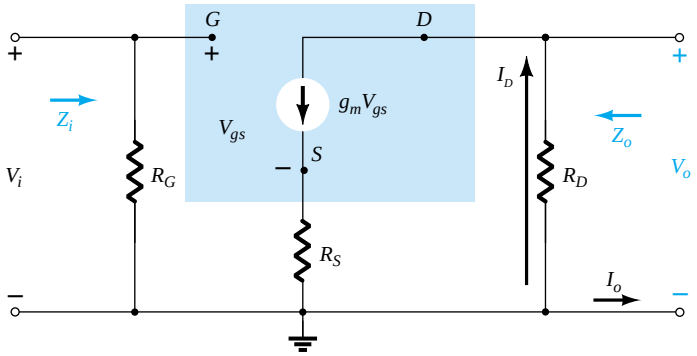


Figure 18 Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i: Due to the open-circuit condition between the gate and output network, the input remains the following:

$$Z_i = R_G \tag{23}$$

Z_o: The output impedance is defined by

$$Z_o = \frac{V_o}{I_o}\Big|_{V_i = 0}$$

Setting $V_i = 0$ V in Fig. 18 will result in the gate terminal being at ground poten- tial (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law will result in:

$$I_o + I_D = g_m V_{gS}$$

with $$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m\,(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $$I_o = -I_D$$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = R_D}\Big|_{r_d = \infty\Omega} \qquad (24)$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 19.

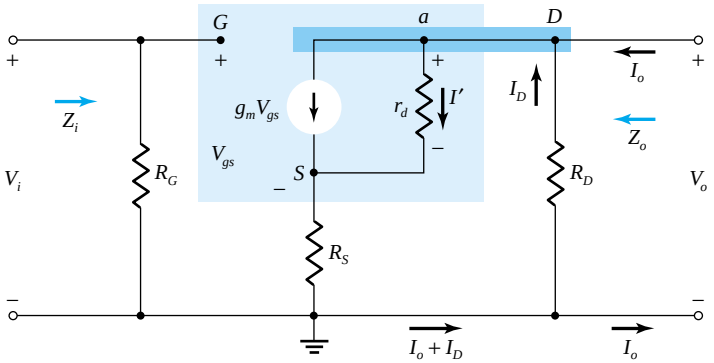


Figure 19 Including the effects of r_d in the self-bias JFET configuration.

Since $$Z_o = \frac{V_o}{I_o}\bigg|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law:

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but $$V_{r_d} = V_o + V_{gs}$$

and $$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or $$I_o = \left(g_m + \frac{1}{r_d}\right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now, $$V_{gs} = -(I_D + I_o)\,R_S$$

so that $$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)\,R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that $$I_o\left[1 + g_m R_s + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or $$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

g_m

and $$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{-I_D\left(1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d}\right)}$$

$$1 + g_m R_S + \frac{R_S}{r_d}$$

and finally, $$\boxed{Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D} \qquad (25a)$$

For $r_d \geq 10\ R_D$, $\left(1 + g_m R_S + \frac{R_S}{r_d}\right) >> \frac{R_D}{r_d}$ and $1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}$ $\cong 1 + g_m R_S + \frac{R_S}{r_d}$ and

$$\boxed{Z_o = R_D}_{r_d \geq 10 R_D} \qquad (25b)$$

A_v: For the network of Fig. 9.19, an application of Kirchhoff's voltage law on the input circuit will result in

$$V_i - V_{gs} - V_{R_S} = 0$$

$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_o - V_{R_S}$$

and $$I' = \frac{V_o - V_{R_S}}{r_d}$$

so that an application of Kirchhoff's current law will result in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S} we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that $$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or $$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

and $$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}} \qquad (26)$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \qquad r_d \geq 10(R_D + R_S) \tag{27}$$

Phase Relationship: The negative sign in Eq. (26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8

The self-bias configuration of Example 6.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is re-drawn as Fig. 20 with an applied signal V_i. The value of y_{os} is given as 20 μS.

(a) Determine g_m.
(b) Find r_d.
(c) Find Z_i.
(d) Calculate Z_o with and without the effects of r_d. Compare the results.
(e) Calculate A_v with and without the effects of r_d. Compare the results.

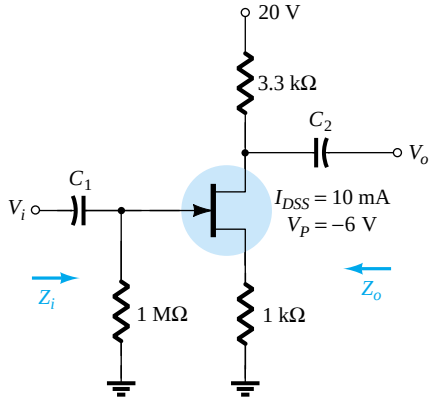


Figure 20 Network for Example 9.8.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$r_d = 50\text{ k}\Omega > 10\,R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\ \Omega$

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

(e) With r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

g_m

Without r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\ \text{mS})(3.3\ \text{k}\Omega)}{1 + (1.51\ \text{mS})(1\ \text{k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d was minimal because the condition $r_d \geq 10(R_D + R_S)$ was satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

IV. VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 9.21.

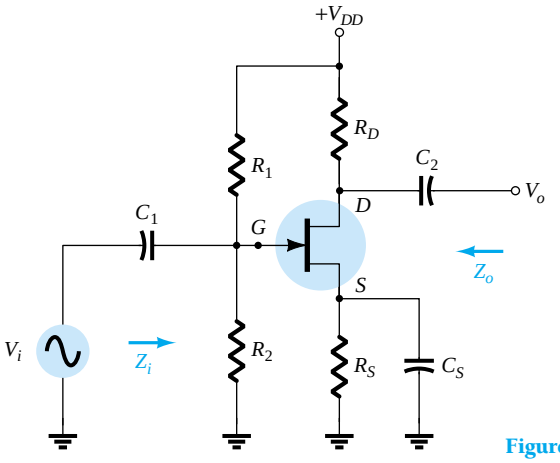


Figure 21 JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET will result in the configuration of Fig. 22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 23. R_D can also be brought down to ground but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

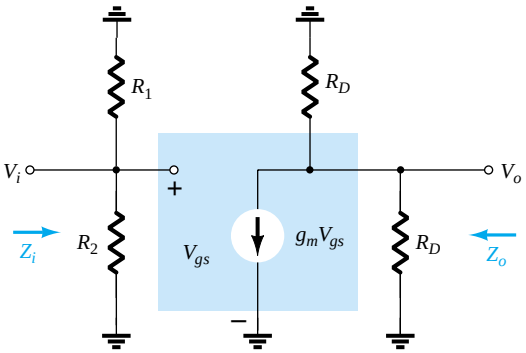


Figure.22 Network of Fig. 21 under ac conditions.

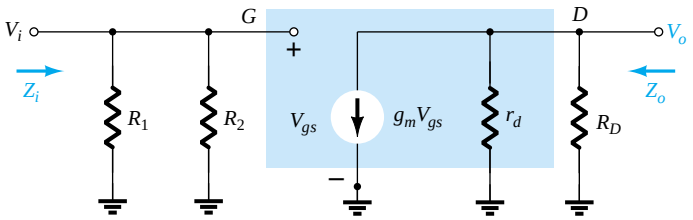


Figure 23 Redrawn network of Fig. .22.

Z_i: R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET resulting in

$$Z_i = R_1 \| R_2 \tag{28}$$

Z_o: Setting $V_i = 0$ V will set V_{gs} and $g_m V_{gs}$ to zero and

$$Z_o = r_d \| R_D \tag{29}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad \text{for } r_d \geq 10R_D \tag{30}$$

A_v:

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{31}$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad \text{for } r_d \geq 10R_D \tag{32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

V. JFET SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 9.24. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology common-drain).

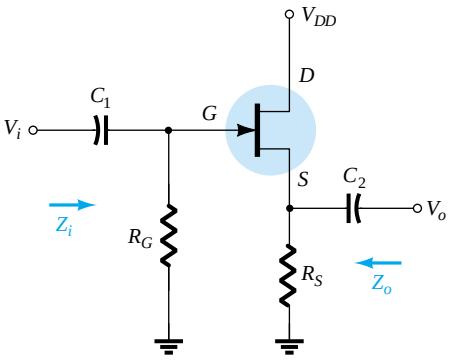


Figure 24 JFET source-follower configuration.

g_m

Substituting the JFET equivalent circuit will result in the configuration of Fig. 25. The controlled source and internal output impedance of the JFET are tied to ground at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to the same terminal and ground, they can all be placed in parallel as shown in Fig. 26. The current source reversed direction but V_{gs} is still defined between the gate and source terminals.

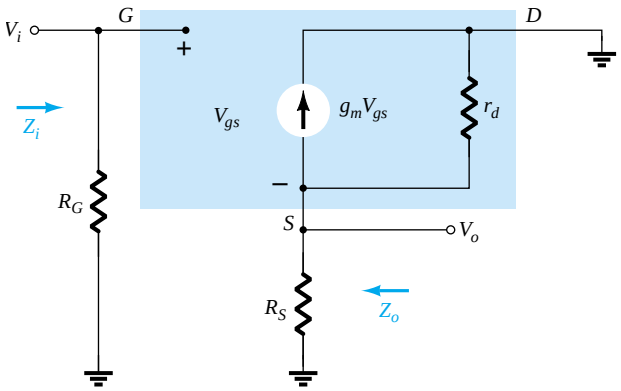


Figure 25 Network of Fig. 24 following the substitution of the JFET ac equivalent model.

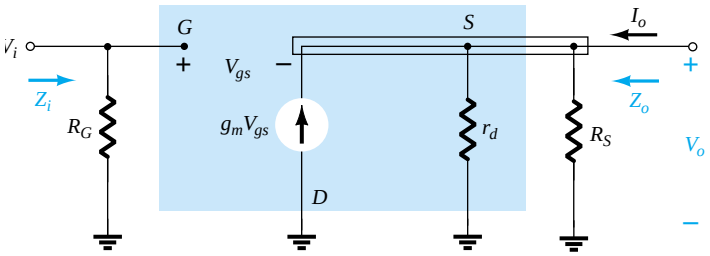


Figure.26 Network of Fig. 25 redrawn.

Z_i: Figure 9.26 clearly reveals that Z_i is defined by

$$Z_i = R_G \tag{33}$$

Z_o: Setting $V_i = 0$ V will result in the gate terminal being connected directly to ground as shown in Fig. 9.27. The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

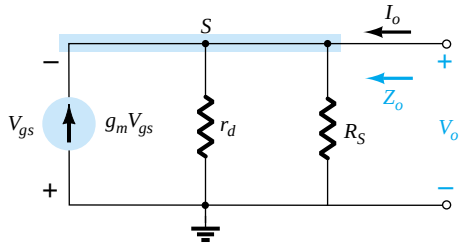


Figure 27 Determining Z_o for the network of Fig..24.

Applying Kirchhoff's current law at node *s*,

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$
$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and $$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{34}$$

For $r_d \geq 10R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{r_d \geq 10R_S} \tag{35}$$

A_v: The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 9.26 will result in

$$V_i = V_{gs} + V_o$$

and $$V_{gs} = V_i - V_o$$

so that $$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or $$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and $$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that $$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{36}$$

In the absence of r_d or if $r_d \geq 10R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}}_{r_d \geq 10R_S} \tag{37}$$

Since the bottom of Eq. (36) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-fol-lower BJT network).

Phase Relationship: Since A_v of Eq. (36) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

EXAMPLE .9 A dc analysis of the source-follower network of Fig. 9.28 will result in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

(a) Determining g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o with and without r_d. Compare results.
(e) Determine A_v with and without r_d. Compare results.

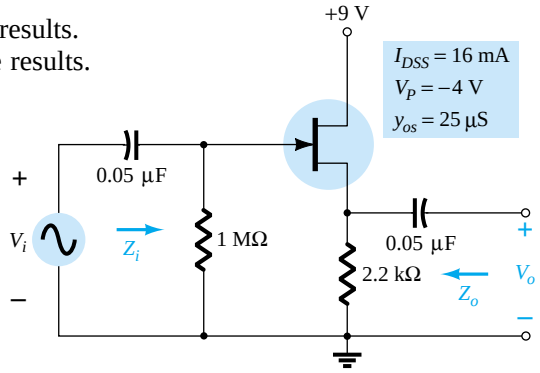


Figure .28 Network to be analyzed in Example .9.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$\begin{aligned} Z_o = r_d \| R_S \| 1/g_m &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS} \\ &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega \\ &= \mathbf{362.52\ \Omega} \end{aligned}$$

revealing that Z_o is often relatively small and determined primarily by $1/g_m$. Without r_d:

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

revealing that r_d typically has little impact on Z_o.

(e) With r_d:

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$

$$\frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1 as predicted above.
Without r_d:

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\text{ mS})(2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.2\text{ k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

revealing that r_d usually has little impact on the gain of the configuration.

VI. JFET COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configura-tion of Fig..29, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit will result in Fig..30. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network. In addition, the resistor connected between input terminals is no longer R_G but the resistor R_S connected from source to ground. Note also the location of the control-ling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

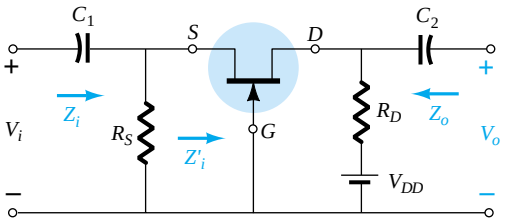


Figure .29 JFET common-gate configuration.

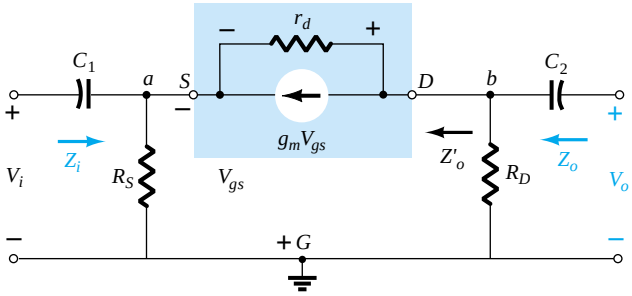


Figure 30 Network of Fig. 9.29 following substitution of JFET ac equivalent model.

***Zi*:** The resistor *Rs* is directly across the terminals defining *Zi*. Let us therefore find the impedance *Zi'* of Fig. 29, which will simply be in parallel with *Rs* when *Zi* is defined.

The network of interest is redrawn as Fig. 9.31. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network will result in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

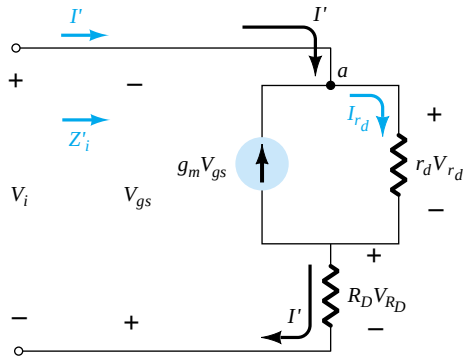


Figure 9.31 Determining Z'

Applying Kirchhoff's current law at node *a* results in

$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

so that

$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and

$$Z'_i = \frac{V'}{I'} = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} \qquad (38)$$

or

$$Z'_i = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

g_m

and $$Z_i = R_S \| Z_i'$$

results in $$\boxed{Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d} \right]} \tag{39}$$

If $r_d \ 10R_D$, Eq. (38) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \frac{R_D}{r_d}\right]}{\left[g_m + \frac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and $$\boxed{Z_i \cong R_S \| 1/g_m}_{r_d \geq 10R_D} \tag{40}$$

Z_o: Substituting $V_i = 0$ V in Fig. .30 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \tag{41}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{42}$$

A_v: Figure 30 reveals that

$$V_i = -V_{gs}$$

and $$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and $$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 30 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and $$I_D = -I_{rd} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that $$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$

$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and $$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \tag{43}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (43) can be dropped as a good approximation and

$$A_v = g_m R_D \quad \text{for } r_d \geq 10R_D \tag{44}$$

Phase Relationship: The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 10

Although the network of Fig. 32 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 29. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Determine V_o with and without r_d. Compare results.

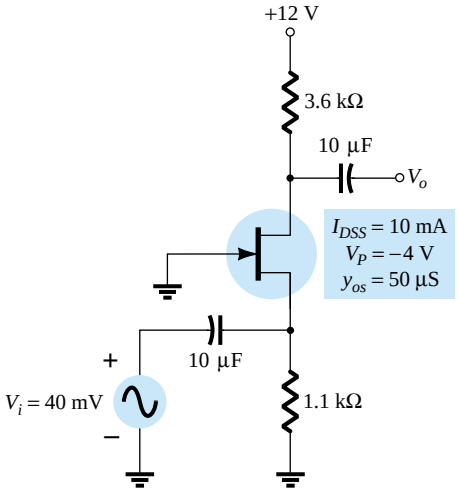


Figure 32

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\ mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{50\ \mu\text{S}} = \mathbf{20\ k\Omega}$$

(c) With r_d:

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ ms})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\ k\Omega}$$

g_m

Without r_d:

$$Z_i = R_S \| 1/g_m = 1.1\ \text{k}\Omega \| 1/2.25\ \text{ms} = 1.1\ \text{k}\Omega \| 0.44\ \text{k}\Omega$$
$$= \mathbf{0.31\ k\Omega}$$

Even though the condition,

$$r_d \geq 10R_D = > 20\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega) = > 20\ \text{k}\Omega \geq 36\ \text{k}\Omega$$

is *not* satisfied, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

(d) With r_d:

$$Z_o = R_D \| r_d = 3.6\ \text{k}\Omega \| 20\ \text{k}\Omega = \mathbf{3.05\ k\Omega}$$

Without r_d:

$$Z_o = R_D = \mathbf{3.6\ k\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

(e) With r_d:

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\ \text{mS})(3.6\ \text{k}\Omega) + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}{\left[1 + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $$A_v = \frac{V_o}{V_i} = \blacktriangleright V_o = A_v V_i = (7.02)(40\ \text{mV}) = \mathbf{280.8\ mV}$$

Without r_d:

$$A_v = g_m R_D = (2.25\ \text{mS})(3.6\ \text{k}\Omega) = \mathbf{8.1}$$

with $$V_o = A_v V_i = (8.1)(40\ \text{mV}) = \mathbf{324\ mV}$$

In this case, the difference is a little more noticeable but not dramatically so.

SUMMARY TABLE

g_m

TABLE 9.1 Z_i, Z_0, and A_v for various FET configurations

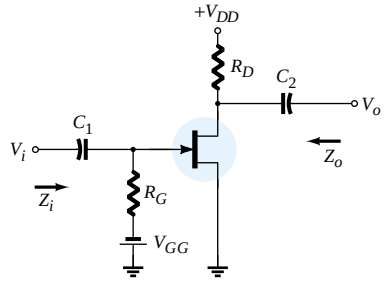
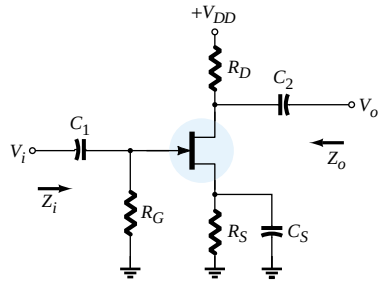
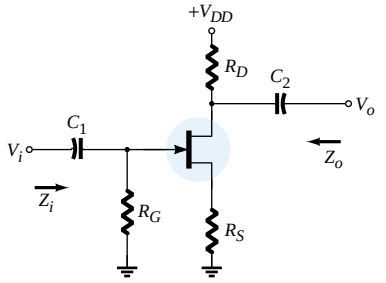
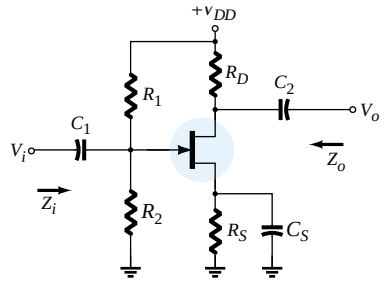
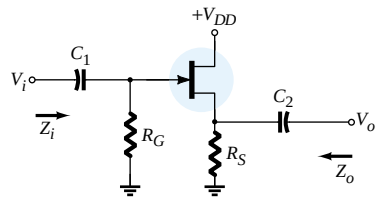
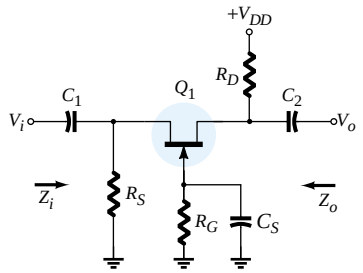
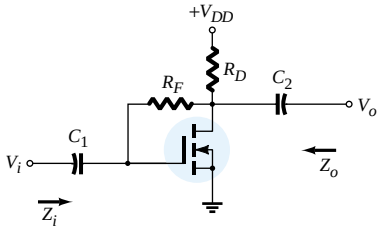
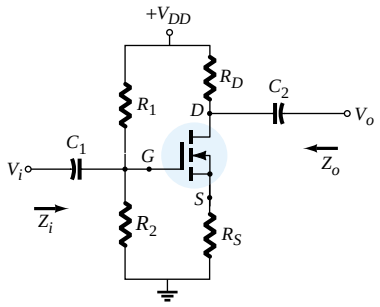
Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_s [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10\,R_D$ or $r_d = \infty\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_s + \frac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_d + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

TABLE 9.1 (Continued)

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m \quad (r_d \geq 10\, R_S)$	Low (< 1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S} \quad (r_d \geq 10\, R_S)$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d} \right] \right.$ $\cong R_S \| \frac{1}{g_m} \quad (r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D \quad (r_d \geq 10\, R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D \quad (r_d \geq 10\, R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$ $\cong \frac{R_F}{1 + g_m R_D} \quad (r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_F \| r_d \| R_D$ $\cong R_D \quad (R_F, r_d \geq 10\, R_D)$	Medium (−10) $= -g_m(R_F \| r_d \| R_D)$ $\cong -g_m R_D \quad (R_F, r_d \geq 10\, R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D \quad (R_d \geq 10\, R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D \quad (r_d \geq 10\, R_D)$